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55497 7590 09/24/2009

VISTA IP LAW GROUP LLP
1885 Lundy Avenue
Suite 108
SAN JOSE, CA 95131

EXAMINER	
GUILL, RUSSELL L	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/24/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,540	08/28/2000	Alexander D. Schapira	CA7010652001	7789

TITLE OF INVENTION: METHOD AND SYSTEM FOR SIMULATION OF DIGITAL/ANALOG INTERFACES WITH ANALOG TRI-STATE IOPUTS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$0	$0	$1510	12/24/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

55497 7590 09/24/2009

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1885 Lundy Avenue
Suite 108
SAN JOSE, CA 95131

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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nonprovisional	NO	$1510	$0	$0	$1510	12/24/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
GUILL, RUSSELL L	2123	703-014000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 907 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 907 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	09/648,540	SCHAPIRA ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an aendment after final filed August 19, 2009*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINERS AMENDMENT

1. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this amendment was given in telephone interview with E. Tzou on September 10, 2009.

3. The claims have been amended as follows:

   a. Claim 5, line 11, the words, "from [[the]]a" have been replaced with --from a--.

   b. Claim 9, line 22, the words, "the computer readable storage device" have been replaced with --a computer readable storage device--.

Allowable Subject Matter

4. Claims 1 - 20 are allowable over the prior art of record.

5. Following is an Examiner's statement of reasons for allowance:

6. Regarding claim 1, while Nair (U.S. Patent 6,090,149) teaches a circuit design simulator with a stored electronic representation of a circuit design, the circuit design including at least one interface between a digital circuit and an analog circuit the interface comprising a node at which said digital circuit provides an output and at which said analog circuit receives an input, neither Nair taken alone or in combination with the prior art of record discloses the aforementioned circuit design simulator specifically including a "circuit design including at least one interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides a digital circuit output and at which said analog circuit receives an

input and provides either an output or no output, said digital circuit output taking on any one of several states including a digital high state, digital low state, or a high impedance state; at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether to apply said output or said no output to said node according to said digital circuit output state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

7. Regarding claim 3, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "a node at which said digital circuit provides an output and at which said analog circuit receives an input, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state", "modeling said output as a digital output signal from said digital circuit to said node when said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output is in said high impedance state; dynamically switching between said digital output signal and said analog output signal based upon whether or not said output is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

8. Regarding claim 5, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair

taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "said interface comprising a node at which each of said plurality of digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state", "modeling at least one of said output as a digital output signal from a corresponding digital circuit to said node when said at least one output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output provided by each of said plurality of digital circuits is in said high impedance state; dynamically switching between said digital output signal and said analog output signal based upon whether or not said plurality of digital circuits is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

9. Regarding claim 8, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electrical operation at an analog/digital interface in a circuit design, neither Nair taken alone or in combination with the prior art of record discloses the aforementioned simulation in a circuit design specifically including "identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit either outputs a digital signal or else presents a high impedance output so as to be effectively isolated from said node, and at which said analog circuit receives an input signal at an input port; adding a conditional output signal from said input port of said analog circuit to said node, wherein either an output signal or no output signal is applied from said analog circuit to said node", and "simulating electrical operation at said interface by applying said output signal from said analog circuit to said node when said digital circuit presents a high impedance

output, and applying said no output signal from said analog circuit to said node when said digital circuit presents a digital signal", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

10. Regarding claim 9, while Nair (U.S. Patent 6,090,149) teaches a method for simulating electronic activity at an analog/digital interface in a circuit design, identifying an interface between a digital circuit and an analog circuit, neither Nair taken alone or in combination with the prior art of record discloses a method for simulating electronic activity at an analog/digital interface in a circuit design, specifically including, "said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state", and "modeling at least one of said output provided by said one or more digital circuits as a digital output signal from a corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output provided by each of said one or more digital circuits is in said high impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

11. Regarding claim 13, while Nair (U.S. Patent 6,090,149) teaches a method for simulating a circuit design, neither Nair taken alone or in combination with the prior art of record teaches the aforementioned method for simulating a circuit design specifically including "identifying an interface between a plurality of digital circuit outputs and an analog circuit input, wherein each of said plurality of digital circuit outputs can present

a high impedance state; modeling said interface by using a processor to add an output from an analog circuit receiving said analog circuit input to said interface", and "simulating electrical operation at said modeled interface by resolving an electrical state of said interface using only the output from the analog circuit when all of said plurality of digital circuit outputs are in a high impedance state, and resolving the electrical state of said interface using one or more of said plurality of digital circuit outputs otherwise", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

12. Regarding claim 14, while Nair (U.S. Patent 6,090,149) teaches a mixed analog/digital simulator, neither Nair taken alone or in combination with the prior art of record teaches the aforementioned mixed analog/digital simulator specifically including "a simulation processor; said simulation processor including a computer-readable medium on which is embodied a set of programmed instructions that cause said simulation processor to simulate the operation of a design circuit, wherein said design circuit includes: (1) a digital circuit having an output; (2) a network electrically coupled to said digital circuit output, said network formed by electrically coupling an input of each of a plurality of circuit blocks at a network input node; (3) said circuit blocks including at least one analog circuit having an analog circuit input electrically coupled to said network input node; (4) said analog circuit having an input mode of operation for receiving an input signal at said analog circuit input and an output mode of operation for producing an output signal at said analog circuit input; (5) said digital circuit output being applied to said network input node when said digital circuit is in a non-high-impedance state; and (6) said output signal of said analog circuit being applied to said network input node when said digital circuit is in a high-impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

13. Regarding claim 17, while Nair (U.S. Patent 6,090,149) teaches a method of simulating mixed analog/digital systems, neither Nair taken alone or in combination with the prior art of record teaches the aforementioned method of simulating mixed analog/digital systems specifically including "transforming an input of an analog circuit into an ioput, said ioput having a conditional output feeding back to a bus, said ioput being operable under a high-impedance input state, and said ioput capable of accepting a digital signal input and producing an analog signal output", "electrically coupling said ioput to a digital circuit output and to inputs of a plurality of additional circuits; receiving said digital signal input at said ioput when said digital circuit output is in a non-high-impedance state; applying said analog signal output at said ioput when said digital circuit output is in a high-impedance state", in combination with the remaining elements and features of the claimed invention. It is for these reasons that the applicant's invention defines over the prior art of record.

14. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L Rodriguez/
Supervisory Patent Examiner,
Art Unit 2123